IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of: Lea Di Cioccio et al. Confirmation No. 3317

Serial No.: 10/526,657 Art Unit: 2822

Filing Date: March 2, 2005 Examiner: Seth W. Barnes

For: METHOD FOR THE PRODUCTIONOF A COMPOSITE SiCOI – TYPE SUBSTRATE COMPRISING AN EPITAXY STAGE

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

In response to the Notice of Non-Compliant Appeal Brief dated June 24, 2008, applicants hereby submit an amended Appeal Brief in support of Notice of Appeal filed November 15, 2007 in the above-referenced application. In particular, applicants added the Evidence Appendix and Related Proceeding Appendix to the Appeal Brief pursuant to 37 CFR 41.37(c). Accordingly, applicants respectfully request consideration of the present application by the Board of Patent Appeals and Interferences.

The response is timely filed and no fee is believed due for this submission.

REAL PARTY IN INTEREST

The real parties of interest are assignees of the present application: Commissariat A L'Energie Atomique and S.O.I.TEC Silicon On Insulator Technologies, French Corporations.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences in connection with this application.

STATUS OF CLAIMS

Claims 1-6 and 12-26 have been canceled.

Claims 7-11 have been finally rejected and are on appeal.

STATUS OF AMENDMENTS

In the Final Office Action dated May 18, 2007, claims 7 and 10-11 were rejected under 35 U.S.C. § 102(a) as being anticipated by Letertre et al., "QuaSIC Smart-Cut Substrates for SIC High Power Devices" (Letertre) and claims 8-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Letertre in view of Vinod et al., "Fabrication of Low Defect Density 3C-SIC on SiO2 Structures Using Wafer Bonding Techniques" (Vinod).

No amendment has been filed subsequent to the Final Office Action.

SUMMARY OF THE CLAIMED SUBJECT MATTER

The invention relates to a method for manufacturing of SiCOI-type composite substrate at temperatures of 1350°C and higher. It is generally acknowledged in the field of solid state electronics that for temperatures of up to 1350°C the quality of 6H and 4H polytype epitaxy on SICOI with silicon support plate is poor and that for temperatures over 1400°C, the oxide will be degraded, i.e. destroyed, or recrystallised. See specification at paragraphs 15. However, the applicants succeeded in carrying out epitaxy at the above conditions and unexpectedly obtained several satisfactory results. The oxide was not degraded at high temperatures (1410°C-1600°C) when the epitaxy was conducted on SiCOI substrates formed from an SiC support successively bearing a silicon oxide layer and a thin SiC layer, making it possible to produce high quality epitaxy. See *Id.* at paragraph 16-17.

Claim 7 recites a method comprising: supplying an initial substrate comprising a SiC support **(1)** bearing a layer **(2)** of SiO_2 whereon a thin layer **(3)** of SiC is transferred, the thin layer **(3)** of SiC being a 6H or 4H polytype SiC (see e.g., paragraph 36 and **Fig. 1**); and conducting an epitaxy of SiC **(4)** on the thin layer **(3)** of SiC at a temperature from 1450°C to 1550°C to obtain 6H or 4H polytype epitaxy **(4)** on the transferred thin 6H or 4H polytype layer respectively (see e.g., paragraph 37 and **Fig. 1**).

Claim 11 recites a semiconductor device produced on an SiCOI composite substrate obtained by means of the manufacturing method according to any of claim 7 (see **Fig. 1**).

GROUND OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 7, 10 and 11 are anticipated under 35 U.S.C. 102(a) by Letertre publication.

Whether claims 8 and 9 are unpatentable under 35 U.S.C. 103(a) over Letertre in view of Vinod publication.

ARGUMENTS

Claims 7-11 are patentable over Letertre and/or Vinod publications.

Claim 7 recites a method for manufacturing SiCOI substrate, the method comprising, inter alia, "supplying an initial substrate comprising a SiC support bearing a layer of SiO_2 whereon a thin layer of SiC is transferred... and conducting an epitaxy of SiC on the thin layer of SiC at a temperature from 1450°C to 1550°C ."

According to the M.P.E.P., a claim is anticipated under 35 U.S.C. § 102(a) only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.[1] Letertre does not disclose all limitation of claim 7.

First, Letertre does not disclose, teach or even suggest SiO_2 as a bonding layer between SiC substrate and the thin layer of SiC. In Introduction on page 151, Letertre mentions that it is known to use oxide layer as a bonding layer between SiC substrate and thin SiC film. The reference, however, does not mention that such oxide layer may be Silicon Oxide (SiO_2) are recited in claim 7 of the present application. Moreover, in next sentence, Letertre proposes a new method for fabricating SiCOI substrate, which does not involve oxide as bonding layer. In contrast, Letertre describes tungsten silicide (WSi_2) as bonding agent of choice, thereby teaching away from the present invention.

Furthermore, Leterter fails to describe epitaxy of SiC on the thin layer of SiC [which are bonded using SiO_2] at a temperature from 1450°C to 1550°C. To that end, applicants state at paragraph 15 of the specification the following:

"The corresponding technical literature does not apparently report on research on 6H or 4H polytype SiC epitaxy on SiCOI substrates. This is due to the fact that it is acknowledged that, for temperatures of up to 1350 °C, the quality of 6H and 4H polytype epitaxy will be poor (case of epitaxy on SICOI with silicon support plate). In addition, over 1400 °C the oxide will be degraded, i.e. destroyed, or recrystallised."

For this reason, the results obtained by the applicants were unexpected, as reported in paragraph 16 of the specification:

"However, the inventors of the present invention succeeded in carrying out epitaxy on all these different types of materials and unexpectedly obtained several satisfactory results. The oxide was not degraded at high temperatures (1410 °C.-1600 °C.) when the epitaxy was conducted on SiCOI substrates formed from an SiC support successively bearing a silicon oxide layer and a thin SiC layer, making it possible to produce high quality epitaxy, comparable to epitaxy on solid sic. The inventors also conducted 6H and 4H polytype SiC epitaxy on SiCOI substrates wherein the support is made of silicon. Encouraging results were obtained."

Accordingly, Leterter fails to anticipate claim 7 of the present application. As to dependent claims 8-11, the argument set forth above is equally applicable here, because dependent claim incorporate all limitations of their base claim 7.

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[1] Manual of Patent Examining Procedure (MPEP) § 2131. See also *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Vinod publication also fails to describe the aforementioned limitations of claim 7 and therefore, does not preclude patentability of the present application.

In view of the foregoing, it is respectfully asserted that the claims 7-11 are in condition for allowance. Favorable disposition to the effect is respectfully requested.

Respectfully submitted,

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CLAIMS APPENDIX

1-6. (Canceled).

7. (Previously Presented) A method comprising:

supplying an initial substrate comprising an SiC support bearing a layer of SiO2 whereon a thin layer of SiC is transferred, the thin layer of SiC being a 6H or 4H polytype SiC; and

conducting an epitaxy of SiC on the thin layer of SiC at a temperature from 1450°C to 1550°C to obtain 6H or 4H polytype epitaxy on the transferred thin 6H or 4H polytype layer respectively.

8. (Previously Presented) The method according to claim 7, wherein before the epitaxy step, an initial substrate preparation step is provided to improve the surface quality of the transferred thin SiC layer.

9. (Previously Presented) The method according to claim 8, wherein the preparation step consists of subjecting the surface of the transferred thin SiC layer to an operation selected from polishing etching and hydrogen etching.

10. (Previously Presented) The method according to claim 7, wherein several SiC layers are successively grown epitaxially on the thin SiC layer.

11. (Previously Presented) A semiconductor device produced on an SiCOI composite substrate obtained by means of the manufacturing method according to any of claims 7 to 10.

12-26 (Cancelled).

EVIDENCE APPENDIX

None.

RELATED PROCEEDING APPENDIX

None.